26. (new) A method for manufacturing a semiconductor device according to claim 25, wherein the second conductive layer is formed from at least one material selected from the group consisting of tungsten, aluminum, copper, titanium silicide, tungsten silicide, cobalt silicide and molybdenum silicide.--

Remarks

This amendment is in response to the Office Action dated November 21, 2002. Claims 1, 3 and 5-17 have been amended and new claims 22-26 have been added. Claims 18-21 were previously canceled without prejudice. Claims 1-17 and 22-26 are currently pending. Reexamination and reconsideration are respectfully requested.

Applicant has amended the specification as requested by the Examiner by inserting the application numbers for the two co-pending applications listed one page 1 of the specification.

Claims 1-17 were rejected under 35 U.S.C. 112, second paragraph. Applicant does not agree with the Examiner that the terms "conduction layer" are indefinite. However, to expedite prosecution, applicant has amended the claims to replace "conduction" with "conductive" as suggested by the Examiner. Applicant respectfully submits that claims 1-17 comply with section 112.

Claims 14-15 were also amended for clarity and not in response to any rejection.

Claims 1-17 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,960,270 to Misra et al. (hereinafter "Misra"). The rejection is respectfully traversed.

Applicant does not agree with the Examiner's characterization of Misra. Applicant respectfully submits that the Examiner has cited no portion of the art that describes or suggests "forming a second conductive layer in the recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer" as recited in claim 1. The

Examiner cited Misra Fig. 17 and reference number 128 in an effort to establish that Misra describes "forming a second conductive layer in the recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer." Office Action at page 4. However, it appears that Fig. 17 of Misra illustrates layer 128b filling the entire region and does not appear to illustrate a gate electrode including "at least the first conductive layer and the second conductive layer" as recited in claim 1. The Examiner cited Misra Fig. 11 and reference number 108 as indicating a first conductive layer. Office Action at page 4. However, Misra Fig. 17 does not appear to include any portion of reference number 108 because this layer appears to have already been completely removed. Therefore, Misra Fig. 17 appears to indicate that the gate electrode does not include earlier formed conductive layer 108 in addition to layer 128b.

The Examiner further cited Figs. 19-22 in an effort to establish that Misra describes "filling a second conduction layer in the recessed section to form a gate electrode that includes at least the first conduction layer and the second conduction layer." Office Action at page 4. As noted by the Examiner, the steps in Figs. 10-16 of Misra are also used in the embodiment described in Figs. 19-22. The Examiner referred to Misra reference number 108 as a "first conduction layer". As seen in Misra Fig. 16, the entire layer 108 is removed. Fig. 19 shows layer 129, which is a different layer from layer 108. The layer 108, which the Examiner referred to as the first conduction layer, appears to no longer exist when the layer 129 is formed.

Accordingly, in view of at least the above, applicant respectfully submits that the Examiner cited no portion of Misra that describes "forming a second conductive layer in the recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer" as recited in claim 1, and thus the rejection of claim 1 should be withdrawn. The rejection of dependent claims 2-6 should be withdrawn for at least the same reasons as claim 1.

With respect to claim 7, applicant respectfully submits that the Examiner has cited no portion of the art that describes or suggests "forming a second conductive layer in the recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer" as recited in claim 7. The Examiner cited Misra Fig. 9 (and reference number 36) in an effort to establish that Misra describes "forming the second conductive layer in the

recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer." Office Action at page 7. The Examiner also cited reference number 28 as a first conductive layer. Office Action at page 6. However, Figs.7-8 appear to show that the entire layer 28b is removed prior to layer 36 being formed. Thus, the Examiner's citations to the art do not appear to describe or suggest "a gate electrode that includes at least the first conduction layer and the second conduction layer" as recited in claim 7. Accordingly, for at least the above reasons, the rejection of claim 7 should be withdrawn. The rejection of dependent claims 8-12 should be withdrawn for at least the same reasons as claim 7.

With respect to claim 13, applicant respectfully submits that the Examiner has cited no portion of the art that describes or suggests "forming a second conductive layer in the recessed section to form a gate electrode comprising the at least part of the first conductive layer and the second conductive layer" as recited in claim 13. The Examiner cited Misra Fig. 21 in an effort to establish that Misra describes "forming a second conductive layer in the recessed section to form a gate electrode comprising the at least part of the first conduction layer and the second conduction layer." Office Action at page 8. The Examiner also cited reference number 108 and Misra Fig. 11 as describing "forming a first conduction layer . . ." However, Fig. 21 does not appear to show reference number 108. It appears that the layer 108 is removed prior to forming layers 129 and 131a shown in Fig. 21. Accordingly, the Examiner's citations do not appear to describe or suggest forming "a gate electrode comprising at least part of the first conductive layer and the second conductive layer" as recited in claim 13. Accordingly, for at least the above reasons, the rejection of claim 13 should be withdrawn. The rejection of dependent claims 14-17 should be withdrawn for at least the same reasons as claim 13.

New dependent claims 22-26 were added. Support for the claims may be found throughout the specification and in the original claims. It is believed that no new matter has been entered. Examination is respectfully requested.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-17 and 22-26 are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application

is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on February 21 ,2003.

Alan S. Raynes — **Feb. 21 , 2003**
Alan S. Raynes **(Date)**

Version With Markings to Show Changes Made

The paragraph at page 1, lines 6-11 was amended as follows:

Applicant hereby incorporates by reference Japanese Application No. 2000-292143, filed September 26, 2000, in its entirety. Applicant hereby incorporates by reference U.S. Application Serial No. 09/963,168 [_____, filed September 26, 2001, listing Yoshikazu Kasuya as inventor, having docket number 15.47/6065,] in its entirety. Applicant hereby incorporates by reference U.S. Application Serial No. 09/963,903 [_____, filed September 26, 2001, listing Yoshikazu Kasuya as inventor, having docket number 15.48/6066,] in its entirety.

Claims 1, 3 and 5-17 were amended as follows:

1. (amended) A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) forming a gate dielectric layer;

(b) forming a first [conduction] conductive layer on the gate dielectric layer;

(c) forming a first upper layer comprising a material different from the first [conduction] conductive layer on the first [conduction] conductive layer;

(d) forming a second upper layer comprising a material different from the first upper layer on the first upper layer;

(e) forming sidewall spacers on side walls of the first [conduction] conductive layer, the first upper layer and the second upper layer;

(f) forming an insulation layer that covers the second upper layer and the sidewall spacers;

(g) planarizing the insulation layer until an upper surface of the second upper layer is exposed;

(h) removing the second upper layer;

(i) removing the first upper layer to form a recessed section between the sidewall spacers; and

(j) forming a second [conduction] conductive layer in the recessed section to form a gate electrode that includes at least the first [conduction] conductive layer and the second [conduction] conductive layer.

3. (amended) A method for manufacturing a semiconductor device according to claim 1, wherein the step (i) is conducted by an etching method, and in the step (i), a ratio of an etching rate of the first upper layer with respect to an etching rate of the first [conduction] conductive layer is two or greater.

5. (amended) A method for manufacturing a semiconductor device according to claim 1, further comprising, after step (i), forming a barrier layer between the first [conduction] conductive layer and the second [conduction] conductive layer.

6. (amended) A method for manufacturing a semiconductor device according to claim 1, further comprising, after step (i), forming a barrier layer between the first [conduction] conductive layer and the second [conduction] conductive layer, and forming the barrier layer between the second [conduction] conductive layer and the sidewall spacers.

7. (amended) A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) forming a gate dielectric layer;

(b) forming a first [conduction] conductive layer on the gate dielectric layer;

(c) forming an upper layer on the first [conduction] conductive layer, at least a lower portion of the upper layer comprising a material different from at least an upper portion of the first [conduction] conductive layer;

(d) forming sidewall spacers on side walls of the first [conduction] conductive layer and the upper layer;

(e) forming an insulation layer that covers the upper layer and the sidewall spacers;

(f) planarizing the insulation layer until an upper surface of the upper layer is exposed;

(g) removing the upper layer to form a recessed section between the sidewall spacers on the [an] upper portion of the first [conduction] conductive layer; and

(h) forming a second [conduction] conductive layer in the recessed section to form a gate electrode that includes at least the first [conduction] conductive layer and the second [conduction] conductive layer.

8. (amended) A method for manufacturing a semiconductor device according to claim 7, wherein the step (g) is conducted by an etching method, and in the step (g), a ratio of an etching rate of at least the lower portion of the upper layer with respect to an etching rate of the at least upper portion of the first [conduction] conductive layer is two or greater.

9. (amended) A method for manufacturing a semiconductor device according to claim 7, wherein the first [conduction] conductive layer is formed from a polysilicon layer.

10. (amended) A method for manufacturing a semiconductor device according to claim 7, wherein the second [conduction] conductive layer comprises a material selected from the group consisting of a metal, a metal alloy and a metal compound.

11. (amended) A method for manufacturing a semiconductor device according to claim 7, further comprising, after step (g), forming a barrier layer between the first [conduction] conductive layer and the second [conduction] conductive layer.

12. (amended) A method for manufacturing a semiconductor device according to claim 7, further comprising, after step (g), forming a barrier layer between the first [conduction] conductive layer and the second [conduction] conductive layer, and forming the barrier layer between the second [conduction] conductive layer and the sidewall spacers.

13. (amended) A method for manufacturing a semiconductor device, the method comprising:

forming a gate dielectric layer;

forming a first [conduction] conductive layer on the gate dielectric layer;

forming an upper layer on the first [conduction] conductive layer, the upper layer comprising a material different from that of the first [conduction] conductive layer;

forming sidewall spacers on side walls of the first [conduction] conductive layer and the upper layer;

removing the upper layer to form a recessed section between the sidewall spacers and above at least part of the first [conduction] conductive layer; and

forming a second [conduction] conductive layer in the recessed section to form a gate electrode comprising the at least part of the first [conduction] conductive layer and the second [conduction] conductive layer.

14. (amended) A method for manufacturing a semiconductor device according to claim 13, further comprising, after [step (g)] the removing the upper layer and prior to forming the second conductive layer, forming a barrier layer [between the first conduction] on the first conductive layer [and the second conduction layer].

15. (amended) A method for manufacturing a semiconductor device according to claim 13, further comprising, after [step (g)] the removing the upper layer and prior to the forming a second conductive layer, forming a barrier layer [between the first conduction] on the first conductive layer and [the second conduction layer, and forming the barrier layer between the second conduction layer and] the sidewall spacers, wherein the barrier layer will be positioned between the first conductive layer and the second conductive layer and between the sidewall spacers and the second conductive layer.

16. (amended) A method for manufacturing a semiconductor device according to claim 13, wherein the first [conduction] conductive layer and second [conduction] conductive layer comprise materials having different compositions.

17. (amended) A method for manufacturing a semiconductor device according to claim 13, wherein the first [conduction] conductive layer comprises polysilicon and the second [conduction] conductive layer comprises a material selected from the group consisting of a metal, a metal alloy and a metal compound.